# DECIPHERING LUT FPGA CONFIGURATION OF THE FINITE STATE MACHINE CREATED WITH QUARTUS II

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**Abstract.** An analysis is given of the setting process of the logical elements based on LUT (Look Up Table) of programmable logic integrated circuit FPGA (Field-Programmable Gate Array) produced by the Altera Corporation. We use the Quartus II system which is delivered free of charge for the training. The process of obtaining of BDF (Block Diagram / Schematic File) of the automat of microprogram control unit is described. The configuration of the logical elements settings is decrypted.

**Keywords:** logic element, programmable logic integrated circuit, Quartus II, setting.